Remarks

In response to Office Action dated September 10, 2004, and following telephone conversation of Oct. 6, 2004, consideration of the following arguments in favor of patentability is respectfully requested and allowance is solicited. Alternatively, if the arguments presented are not persuasive and because the present Response is filed within 2 months of the mailing of the most recent Office Action, an Advisory Action pointing out specific flaws in Applicant's argument is respectfully requested to better prepare the issues for Appeal.

Applicant thanks Examiner Shrader for his time for telephone conversation of October 6, 2004 helping to clarify the position taken in the Office Action.

Claim 1 is rejected as anticipated by US Pat. No. 5,991,868 to Kamiyama (herein "the Kamiyama patent"). A proper anticipation rejection requires that all elements and limitations of a claim be taught in the prior art. The anticipation rejection is specifically traversed. Applicant understands the position indicated on page 14 of the Office

Action to be that the program status word 106 disclosed in the Kamiyama patent is the same as Applicant's recited element of "a flag selection memory, capable of being programmed with a plurality of selection values, each selection value providing independent selection input into a respective plurality of first flag selectors". In reply, Applicant agrees that the program status word 106 disclosed in the Kamiyama patent is a memory structure. Applicant disagrees that the PSW 106 in the Kamiyama patent teaches all elements and limitations of the flag selection memory as recited in claim 1. In support of Applicant's position, Applicant understands after careful reading of the Kamiyama patent teachings, that the PSW 106 is the source of the flags used for branching. See Col. 4, lines 13-17 of the Kamiyama patent and the fact that FIGURE 6 shows a source of the PSW 106 being calculator 104. Specifically, the Kamiyama patent teaches that *"The flags are stored in eight registers of 1-bit length each in PSW 106"*. Claim 1 recites a "flag selection memory… programmed with… selection values" where "each… value provides independent selection input into a respective plurality of first flag selectors". As a first

point, the Kamiyama patent does not teach that the PSW 104 is programmed with values. See page 22 lines 19-25 of the Specification teaching that contents of the flag selection memory are loaded prior to test program execution. By contrast, the PSW 106 merely receives a fixed number of flags from the calculator 104 during program execution. See col. 4, lines 7-10. As a second point, the Kamiyama patent does not teach that the value in the flag selection memory is a value that determines which flag of the available flags is used. See p. 22, lines 5-7 of the Specification where it is taught "the selection value loaded into the flag selection memory selects one flag from a set of available flags" and claim 1 language "each...first flag selector presenting at an output a...selected flag from a plurality of available flags". By contrast Kamiyama teaches that the PSW 104 contains the flags. See col. 4, lines 13-17 and FIGURE 6. As a third point, the Kamiyama patent does not teach "independent selection input" because input to multiplexing elements 6-1 through 6-4 is a value designating whether flags from an 8-bit or 16-bit flag group are presented to the condition judging unit 7. The determination appears to come from the

conditional instruction itself during execution of the program. Because the flags are selected as a group, the selection is not independent selection, and because the selection is made as part of the instruction, it is not stored in a flag selection memory. As a fourth point, if 6-1 through 6-4 are viewed as first flag selectors, then the Kamiyama patent does not teach "a respective plurality of first flag selectors" because there are eight flags and four first flag selectors disclosed. Additionally, a modification of Kamiyama to a respective plurality serves to negate the 8-bit vs. 16-bit designation. In summary, the Kamiyama patent does not teach or suggest "programmed... selection values...providing independent selection input into a respective plurality of first flag selectors" as claimed. An illustration of the indirect nature of the flag selection according to the present teachings is illustrated in FIGURE 5, where flag selection registers 502 are programmed with values that determine which flag from a plurality of available flags 25, 55 is presented to a second flag selector 506. By contrast, only rudimentary direct flag selection is taught in the Kamiyama patent after designation by the instruction of an 8-bit or

16-bit flag group. For these and other reasons, anticipation is not shown. Claim 1 is believed to be patentable over the Kamiyama patent and withdrawal of the anticipation rejection is respectfully requested. Allowance is solicited. Alternatively, it is requested that specific flaws in Applicant's arguments are pointed out in the Advisory Action to better prepare the issues for Appeal.

Claim 12 is rejected as obvious over US Pat. No. 6,546,550 to Ogata (herein "the Ogata patent") in view of the Kamiyama patent. The Office Action position is that art that teaches dynamic compiler execution, but does not have teachings with respect to flag selection values, in combination with the teachings of the Kamiyama patent renders claim 12 obvious because teachings with respect to a compiler combined with the Kamiyama teachings would suggest the compiler of claim 12 to one of ordinary skill in the art. A proper obviousness rejection requires all elements and limitations of the rejected claim be present or suggested in the combination of the prior art together with a suggestion or motivation to combine to arrive at the claimed invention. Neither the Kamiyama patent nor the Ogata patent

teaches use of a flag selection value. Neither the Kamiyama patent nor the Ogata patent teaches "identifying a flag selection value... and storing... said flag selection value in a respective one of two or more flag selection register array elements" as claimed. Neither the Kamiyama patent nor the Ogata patent teaches use of "two or more flag selection register array elements" as claimed. Because all elements and limitations are not disclosed in the cited prior art, it is not possible for the combination of the two to render obvious the compiler of claim 12. For these and other reasons, there is no basis for a prima facie case of obviousness and withdrawal of the obviousness rejection is respectfully requested. Allowance is solicited. Alternatively, it is requested that specific flaws in Applicant's arguments are pointed out in the Advisory Action to better prepare the issues for Appeal.

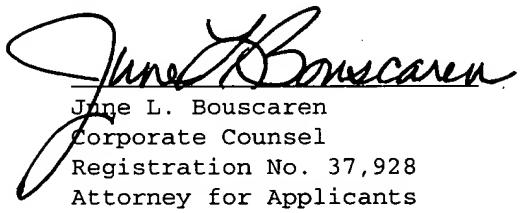
Claim 15 is rejected as obvious over US Pat. No. 4,742,466 to Ochiai (herein "the Ochiai patent") in view of the Kamiyama patent. The position taken in the Office Action is that the Ochiai patent that teaches a compiler for conditional branch instructions that teaches setting a branch/through

flag, but does not have teachings with respect to flag selection memory and the relationship to flag selection values in combination with the teachings of the Kamiyama patent renders claim 15 obvious. Neither the Kamiyama patent nor the Ochiai patent teaches a flag selection memory. Therefore, neither the Kamiyama patent nor the Ochiai patent teaches "a compiler assigning… values for a flag selection memory" as claimed. Additionally, neither the Kamiyama patent nor the Ochiai patent teaches a "flag selection memory capable of being programmed with a plurality of selection values where the values provide independent selection input into …first flag selectors" as claimed. Accordingly, it is not possible for the combination of the two patents to render obvious the apparatus comprising a compiler as claimed and a prima facie case of obviousness is not established. Allowance is solicited. Alternatively, it is requested that specific flaws in Applicant's arguments are pointed out in the Advisory Action to better prepare the issues for Appeal.

If any clarifications can be made by way of telephonic interview, the Examiner is invited to contact the Undersigned.

Respectfully submitted,

Krech et al.
Applicant(s)



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